REMARKS

Claims 8, 10 and 21-23 are pending in the application with the present amendments. In the Office Action, all claims were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,481,120 to Mochizuki et al. ("*Mochizuki*"), or, alternatively, under 35 U.S.C. §103(a) as being obvious over *Mochizuki* in view of U.S. Patent No. 6,287,930 to Park ("*Park*"). For the reasons set forth below, applicants respectfully submit that the presently pending claims are fully distinguished from the references cited by the examiner to reject the claims.

As now recited in claim 8, the bipolar transistor (e.g., transistor 200 (FIG. 10)) includes a first dielectric region (e.g., remaining portion of region 236 (FIG. 11)), the first dielectric region being laterally adjacent to the emitter (e.g., emitter 204). The bipolar transistor further includes a second dielectric region, e.g., the remaining part of dielectric region 250 (FIG. 11), disposed laterally adjacent to the collector pedestal (e.g., collector pedestal 213, FIG. 10). An opening, e.g., opening 250 (FIG. 12), extends through the first and second dielectric regions and has a wall extending through the first and second dielectric regions. As described in the specification, the opening is defined by a reactive ion etch in accordance with a single photolithographic pattern (paragraph [0055]), such process producing the opening having the wall extending through the first and second dielectric regions. The emitter 204 has an edge referenced to a wall of the opening, as is apparent by the fact that an edge of the emitter is spaced from the wall by the width of spacer 231. The collector pedestal 213 has an edge 209 (FIG. 13) referenced to the wall

of that same opening, as described in paragraph [0057]. The recited structure results in advantages as described in paragraph [0053] of the Specification, namely, alignment of the emitter with the collector pedestal, without having to be concerned about lithographic overlay tolerance.

By contrast, at best *Mochizuki* teaches formation of a different opening in a dielectric region 25 (FIG. 25) than the opening already formed in dielectric region 4 (FIGS. 10, 25). *Mochizuki* does not teach a wall of an opening that extends through a first dielectric region and a second dielectric region, to which an edge of the emitter and an edge of the collector pedestal are referenced.

Claims 21 through 23 each recites one or more features which further distinguish the invention from the devices described in *Mochizuki* or the combination of *Mochizuki* and *Park*.

Specifically, claim 21 now recites that the shallow trench isolation is filled with a dielectric. By contrast, the isolation regions 79 (FIG. 3) shown in *Park* are filled with polysilicon rather than a dielectric.

Claim 22 now recites that a wall of the raised portion of the extrinsic base is aligned with a wall of the opening in the first and second dielectric regions. FIGS. 11 and 12 illustrate the alignment of the polysilicon layer 218 which will become this raised portion with the opening 250 in the first and second dielectric regions 236, 270. As neither *Mochizuki* nor *Park* teach such opening having the characteristics recited in claim 8, neither reference teaches alignment of a wall of a raised portion of an extrinsic base with such

opening.

Claim 23 recites a solid dielectric spacer which spaces a raised portion of the extrinsic base, e.g., polysilicon layer 218 (FIG. 11) from the emitter, the solid dielectric spacer including (a) a first dielectric spacer, e.g., a spacer 231 (FIG. 10), wholly contacting a wall of the raised portion of the extrinsic base, and (b) a second dielectric spacer, e.g., spacer 230, contacting an inner wall of the first dielectric spacer remote from the raised portion of the extrinsic base. The combination of *Mochizuki* and *Park* fails to teach dual dielectric spacers having characteristics as recited in claim 23. At best, Park (FIGS. 1-3, 13) shows a polysilicon base 79 (FIG. 3) spaced from the emitter electrode 80 by a single spacer 85.

This amendment is filed together with a petition for a one-month extension of time. It is believed that no other fee is due in connection with the filing of the present response. However, if any fee is due, please debit the Deposit Account No. 09-0458 of the Assignee International Business Machines Corporation.

Respectfully submitted,
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